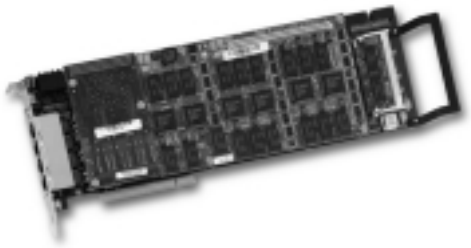
Datasheet

Intel® Dialogic® DM/V480-2T1-PCI-HiZ and DM/V600-2E1-PCI-HiZ Line Tapping Boards

High-Impedance T-1/E-1 Interfaces for Call Logging Applications



The Intel® Dialogic® DM/V480-2T1-PCI-HiZ and DM/V600-2E1-PCI-HiZ line tapping (digital HiZ) boards provide a powerful set of features that developers can use to create call logging systems. Offered on a single-slot, PCI-format board, each digital HiZ board provides call recording capability for two T-1 (1.544 Mb/s) or E-1 (2.048 Mb/s) digital interfaces.

Powerful digital signal processors (DSPs) provide a rich set of voice processing features, including various rates of voice compression, recording, telephony tone signaling, and reliable dual-tone multifrequency (DTMF) detection.

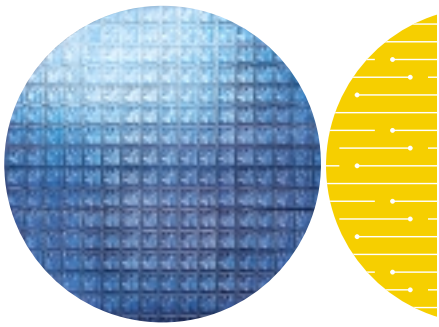
These boards are based on the Intel Dialogic DM3 architecture, which provides an environment that accelerates application development and offers a path for future growth. A software development kit (SDK) is available for Windows NT*, Windows* 2000, and Windows XP operating systems.

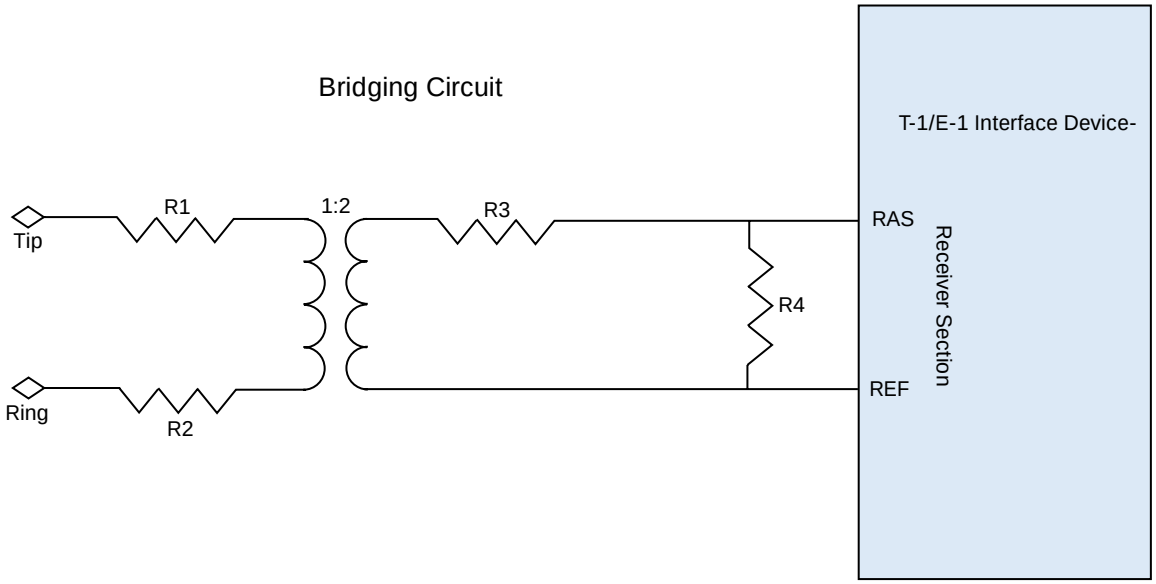
The boards are accompanied by software that monitors trunk signaling to determine the moment a call is set up, connected, and disconnected. This information is used to determine when to start recording the call, as well as to collect Automatic Number Identification (ANI) and Dialed Number Identification Service (DNIS) information. ISDN signaling is supported.

Intel in Communications

Features and Benefits

- Supports two digital trunks per board for recording up to 60 voice channels
- High-impedance interface allows undetectable call monitoring
- Choice of T-1 or E-1 digital network interfaces supporting ISDN PRI protocol
- New call logging interface shortens application development time
- Determines call status and abstracts protocol-specific information for simple application deployment
- Built on the Intel® Dialogic® DM3 architecture for unmatched performance and reliability





Bridging Circuit Used in the Digital HiZ Assembly

These line tapping voice products provide the following functionality in real time on all 48 (T-1) or 60 (E-1) channels:

- monitors trunk signaling and reports to application
- determines when call has been established
- digitally compresses and records voice signals
- detects DTMF signals
- records both sides of a conversation (transaction record)

High-Impedance Line Tap Interface

The digital HiZ assemblies provide a high-impedance tap of T-1 and E-1 trunks for use in call logging systems. The high-impedance tap is achieved by creating a bridging circuit across the T-1 or E-1 trunk and the line tapping board. The bridging circuit resides on the digital HiZ board. A line tap is an electrical coupling to the link signals that connect two communication points. While the link is transparent to the parties involved in the connection, it allows extraction of signaling/protocol information from the network interface.

The bridging circuit presents an impedance to the T-1 and E-1 signals that is approximately 10 times more than the impedance of the line (i.e., 1000 Ohm for T-1 lines, 1200 Ohm for E-1 lines). By presenting this high impedance, the original signal is basically undisturbed.

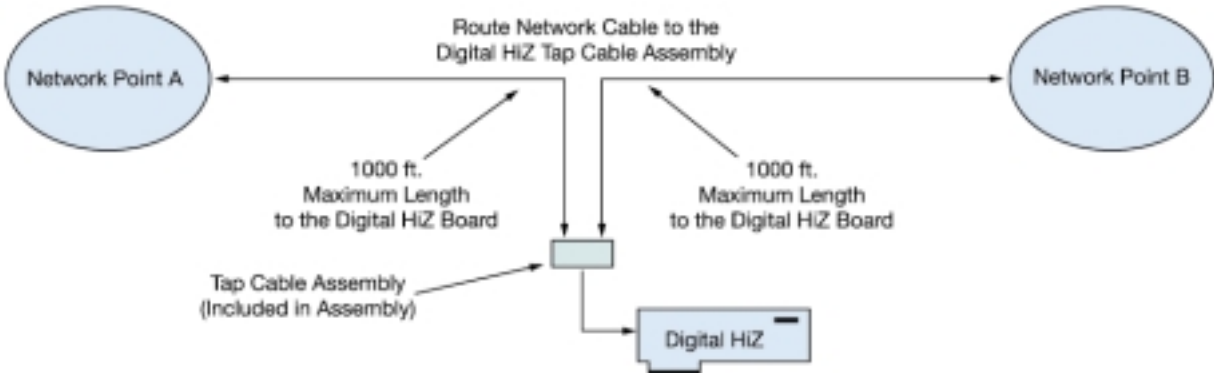
This diagram shows the bridging circuit used in the digital HiZ assembly. The impedance presented by R1, R2, R4, and the transformer to the T-1 and E-1 signals is approximately 1000 Ohm and 1200 Ohm respectively. Four T-1/E-1 interface devices are used in the digital HiZ assembly; the transmit and receive tip and ring pairs of a single trunk are handled by two interface devices.

Downloadable Firmware

The board hardware consists of a baseboard with a RISC processor and four DS1 digital network interfaces for monitoring up to two trunks. (Different assemblies are used for T-1 and E-1.) An array of DSPs resides on a low-profile daughterboard. Telephony signaling protocols and voice processing features are downloaded to the board on power up, and reside as firmware on the various onboard processors, enabling easy feature upgrades and expansion. Individual firmware components, such as a network interface protocol or a voice recording function, are referred to as resources.

Applications

- Call logging
- Call recording
- Call monitoring
- Large end call centers



Supported Configuration

Network Interface

The boards present a high-impedance interface to the digital line (T-1 or E-1).

- The T-1 version (DM/V480-2T1-PCI-HiZ) is fully compatible with all digital interfaces that use, or can be set to use, 1.544 MHz clocking and µ-law pulse code modulation (PCM). The board also supports all T-1 robbed-bit signaling protocols and is fully compatible with all resource devices that use, or can be set to use, µ-law PCM. The DM/V480-2T1-PCI-HiZ board also supports ISDN PRI. The T-1 protocol implementations comply with the North American standard ISDN PRI and the INS-1500 standard used in Japan. In North America and Japan, the ISDN Primary Rate includes 23 voice/data channels (B channels) and one signaling channel (D channel).
- The E-1 version (DM/V600-2E1-PCI-HiZ) is fully compatible with all digital interfaces that use, or can be set to use, 2.048 MHz clocking and A-law PCM (ITU-T Recommendation G.703/704/711). The E-1 boards also support the clear channel feature, thus providing up to 124 bearer channels when used in this mode. The E-1 protocol implementations comply with the E-1 ISDN PRI protocols. The E-1 ISDN Primary Rate includes 30 voice/data channels (B channels) and two additional channels: one signaling channel (D channel) and one framing channel to handle synchronization. Q.SIG protocols for European trunks are also supported.

The digital HiZ boards support ISDN Primary Rate Interface (PRI) access. PRI lets applications take advantage of the speed, power, and flexibility of ISDN. Intel maintains an extensive number of product approvals in the international marketplace. Review the list at http://resource.intel.com/globalapproval/globalapproval.asp.

Voice Processing

Voice processing features, downloaded to the onboard DSPs at power up, let the boards record voice messages from the calling and called parties. Messages can be stored using G.711 µ-law or A-law PCM, at a rate of 64 Kb/s, as is used by the public telephone network. To reduce storage requirements, voice coding algorithms can compress recordings to 24 Kb/s or 32 Kb/s, using adaptive differential pulse code modulation (ADPCM). Other standards-based low-bit-rate coders like (16 Kb/s to 40Kb/s) G.726 for VPIM-compliant applications and (13 Kb/s) 6.10 GSM for unified messaging applications are also available.

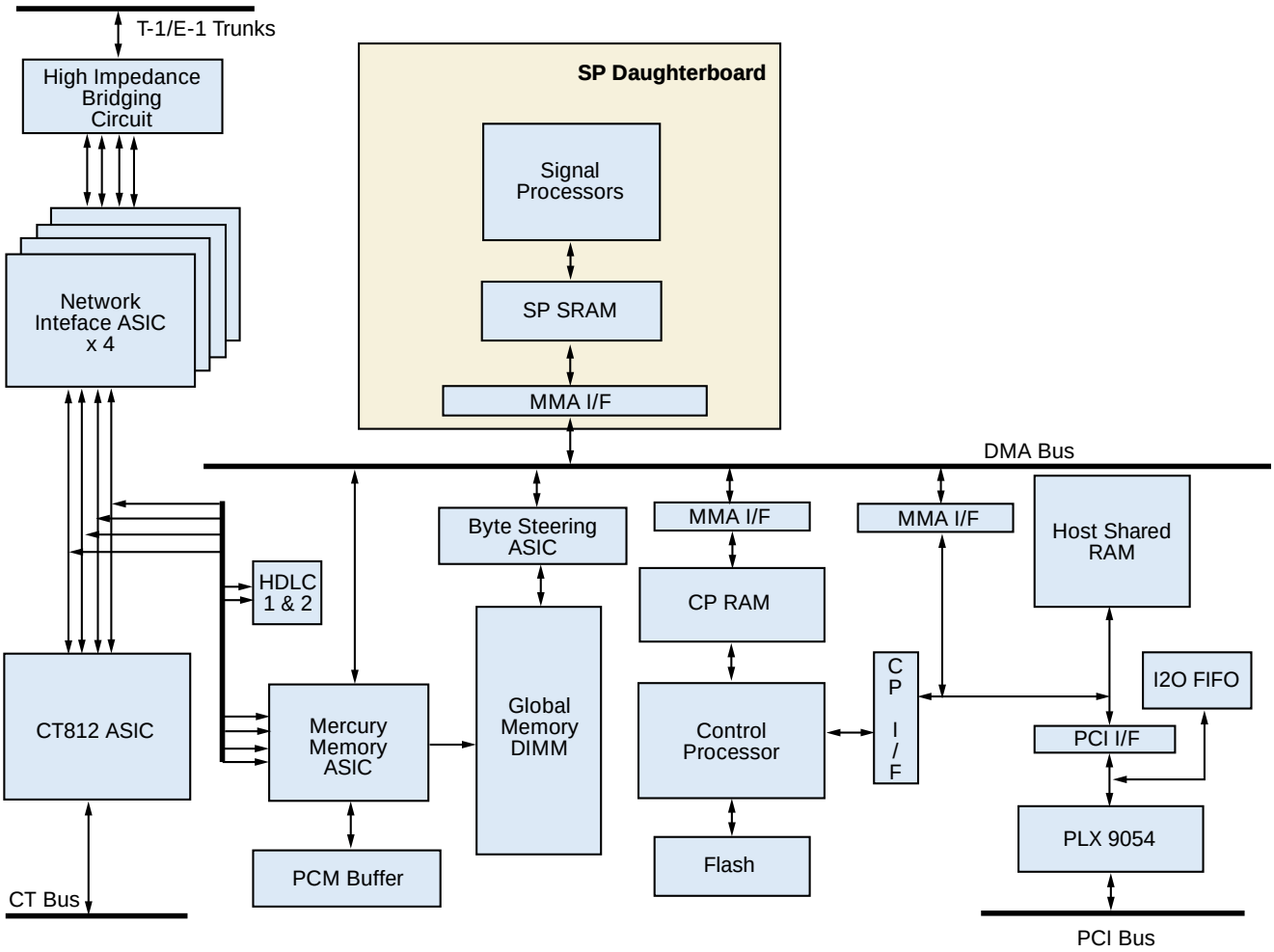
Software Support

These boards are supported with an SDK for Windows NT, Windows 2000, and Windows XP operating systems and contain a complete set of tools for developing complex multichannel call logging applications. In addition, the Intel® NetMerge™ CT Application Development Environment tool supports these boards.

Configurations

The digital HiZ assembly provides tap cables that bring transmit and receive signals to the assembly and lets the signals continue to their destinations. The length of this cable has been carefully designed to minimize reflections; long tap cables must not be used. This configuration diagram illustrates the correct connection to the digital HiZ assembly and the associated trunk lines.

- This is the recommended configuration for use with the digital HiZ boards.
- The short tap cable assembly is included with the digital HiZ assembly; see the quick install card at http://resource.intel.com/telecom/support/Install/Config/DM3/1559-1.pdf.



Functional Description

- The network cable needs to be brought to the digital HiZ board tap cable assembly.
- The tap cable assembly was designed to provide a short tap to the digital HiZ card and to let the tapped signal continue to the destination.
- The board can be placed anywhere along the network cable, using the small tap cable assembly, to a maximum length of 1000 ft (300 m) from any one of the network terminating points.
- The T-1 (DM/V480-2T1-PCI-HiZ) board configuration was tested successfully with 1000 ft (300 m) of 100 Ohm shielded T-1.
- The E-1 (DM/V600-2E1-PCI-HiZ) board configuration was tested successfully with 1000 ft (300 m) of 120 Ohm shielded E-1.
- Note: Using Ethernet CAT5 cable to connect to T-1 or E-1 boards is not recommended for long distance line tapping.

Functional Description

The DM/V480-2T1-PCI-HiZ and DM/V600-2E1-PCI-HiZ boards are based on the DM3 architecture. The architecture consists of a set of core specifications and firmware modules that are implemented on boards with various processors, including

- RISC processor for centralized control
- DSP(s) for mediastream processing
- TDM bus interface (H.100/H.110)
- Digital telephony network interfaces
- PCI bus interface

The DM/V480-2T1-PCI-HiZ and DM/V600-2E1-PCI-HiZ boards support up to 48 (T-1) or 60 (E-1) channels of voice processing via a bank of DSPs and up to four T-1 or E-1 digital trunk interface (DTI) circuits. The DTI circuits contain signaling services (ISDN and Common Channel Signaling), plus any alarm handling and line

maintenance services required by the installed networks. Each DTI includes software switchable clock circuits that can be set to

- Loop (clocking is slaved to the external network)
- Independent (clocking is derived from an onboard oscillator)
- Expansion or system (clocking is slaved to the TDM; receive clocking is always slaved to the trunk interface)

The control processor is a general-purpose Intel i960® microprocessor, responsible for the initialization, configuration, and control of the various elements that make up the DM/V480-2T1-PCI-HiZ and DM/V600-2E1-PCI-HiZ board products. It controls the TDM bus interface, as well as the signaling protocols for the DTIs installed on the platform.

The DM/V480-2T1-PCI-HiZ and DM/V600-2E1-PCI-HiZ boards support various DSP configurations for voice processing and call progress analysis capabilities. These features are provided by a daughterboard configuration, using up to 10 Motorola* 56311 DSPs per board. The DSPs process the digitized voice data using downloaded resource firmware.

Each DSP can perform the following signal analysis and operations on this incoming data:

- Performs automatic gain control (AGC) to compensate for variations in the level of the incoming audio signal
- Applies ADPCM, PCM, LinearWAV, GSM, and G.726 algorithms to compress the digitized voice and save disk storage space
- Detects the presence of tones: DTMF, MF, or application-defined single or dual tones
- Detects silence detection to determine whether the line is quiet and the caller is not responding

While recording speech, the DSP can use different digitizing rates from 85 Kb/s to 176 Kb/s, as selected by the application for the best speech quality and most efficient storage. The digitizing rate is selected on a channel-by-channel basis, and can be changed each time a record or play function is initiated. The DSP processed speech is transmitted by the control processor to the host PC for disk storage. When playing back a stored file, the processor retrieves voice information from the host CPU and passes it to the DSP, which converts the file into digitized voice. The DSP sends the digitized voice responses to the caller via the network interface or TDM bus.

Shared RAM on the DM/V480-2T1-PCI-HiZ and DM/V600-2E1-PCI-HiZ boards enables communication between the host system and the i960 control processor. A bank of global memory is also provided to facilitate communications between the control processor and the various DSPs. In addition to providing a data pathway between processors, the global memory can also serve as a repository for data that is to be shared among processors, or which may not be storable within local memory associated with the processor.

Functions

The Intel Dialogic DM/V480-2T1-PCI-HiZ and DM/V600-2E1-PCI-HiZ boards provide the following functionality in real time for up to 60 channels per board:

- Connect to 48 (T-1) or 60 (E-1) telephone channels via DSX-1 T-1 termination or CEPT E-1 termination
- Record voice messages in different formats such as linear, OKI ADPCM, G.711 PCM GSM, G.726
- Automatically answer calls using virtually any international telephony signaling protocol
- Automatically track call progress
- Detect touch-tones

Intel maintains an extensive number of product approvals in international markets. See the list of globally approved products at http://resource.intel.com/globalapproval/globalapproval.**asp**.

Voice Processing

Voice processing features, downloaded to the onboard DSPs at power up, let the DM/V480-2T1-PCI-HiZ and DM/V600-2E1-PCI-HiZ boards record voice messages to and from callers through the digital network interface. Messages can be stored using G.711 µ-law or A-law PCM, at a rate of 64 Kb/s, as is used by the PSTN. To reduce storage requirements, voice coding algorithms can compress recordings as low as 8.5 Kb/s using low-bit rate coders such as GSM and G.726. Sampling rates and coding methods are selectable on a channel-by-channel basis. Applications can dynamically switch sampling rate and coding method to optimize data storage or voice quality as needed.

AGC is provided to automatically adjust the signal level of incoming calls for recording at normal levels compensating for adverse line conditions, distance, and other factors.

Tone Signaling

In addition to the DTMF signaling commonly used for voice processing, the DM/V480-2T1-PCI-HiZ and DM/V600-2E1-PCI-HiZ boards also contain a robust set of features used for network tone signaling and control. The global tone detection (GTD) and global tone generation (GTG) features provide the capability to detect and generate user-defined tones for solving special application situations, such as integration with PBX or dealing with unique tones.

Perfect Call, call progress analysis, accurately monitors outbound calls, detects when calls are answered, and distinguishes:

- line ringing with no answer
- line busy
- problem completing call (such as operator intercept)
- call answered by a human or answering machine
- call answered by a fax machine or modem

Perfect Call is intelligently tolerant of the wide variation in call progress signaling tones found in central offices and PBXs around the globe and offers accurate performance right out of the box. DSP-based algorithms are used to accurately discriminate human speech from recorded human voice and from network noise.

System Management

- **Configuration management** — includes features like plug-and-play configuration, individual board validation, automatic addressing, and automatic board configuration to decrease the likelihood of procedural errors caused by inexperienced personnel
- **Performance management** — detailed monitoring at the port, DSP, or board level lets administrators balance system capacity and plan for future growth
- **SNMP** — SNMP-enabled CT components lower the cost of ownership. You can integrate SNMP into an existing infrastructure, or deploy a standard, off-the-shelf SNMP management platform. Remote monitoring and configuration are possible at the board, network, or port level.

Clock Fallback

A fallback clock is provided on a separate board to provide redundancy in case of clock failure. In the event that the master clock fails, the fallback clock takes over to prevent any loss of data. An alarm message is generated in the system log, without interrupting service.

Technical Specifications**

Configuration

Digital interfaces	Two T-1 or two E-1 (two connectors used per T-1/E-1 trunk)
Max. boards/system	Six boards per chassis
Control processor	Application, call traffic, and CPU dependent Intel® i960CF at 33 MHz, 66 MIPs
Control processor memory	Up to 8 MB local to control processor
Digital signal processors	Motorola 56311, 1 K word program cache, Internal Program memory (64k, 1K cache, and Internal Data Memory (64k) Up to 10 DSPs @ 150 MIPs each
DSP memory	512 K word SRAM local to each DSP
Baseboard global memory	32-bit wide DRAM accessible to all signal processors, control processor, and host

PCI Platform

Form factor	PCI long card, single-slot width
Host interface memory	512 KB
Bus compatibility	Rev 2.2 of PCI Bus Specification
Bus mode	Target and DMA master mode operation
Network connectors	Four RJ-48C on rear bracket

Power Requirements†

Configuration		+5 VDC	+12 VDC	–12 VDC	+3.3 VDC
	DMV6002E1PCIHIZ	20 W	N/A	N/A	N/A
	DMV4802T1PCIHIZ	20 W	N/A	N/A	N/A
Operating temperature					
	50°C	2.3 CFM per board			
	40°C	1.5 CFM per board			
	30°C	1.1 CFM per board			
Storage temperature	–20°C to +70°C				
Humidity	8% to 80% non-condensing				

Safety and EMI Certifications

Approvals	For country-specific approval information, see the Global Product Approvals list at http://resource.intel.com/globalapproval/globalapproval.asp
Estimated MTBF	PCI: 96,000 per Bellcore* Method I
Warranty	Intel® Telecom Products Warranty Information at http://www.intel.com/network/csp/jproducts/3144web.htm

†These power requirements are for the platforms with six Motorola 56311 DSPs. Consult your Intel technical sales representative for the power requirements of your specific configuration.

Resource Technical Specifications**

Audio Signal		
	Usable receive range	–40 dBm0 to 0 dBm0 nominal, configurable by parameter‡
	Automatic gain control	Application can enable/disable. Above –21 dBm results in full-scale recording, configurable by parameter.‡
	Silence detection	–40 dBm nominal, software adjustable‡
	Transmit level (weighted average)	–12.5 dBm0 nominal, configurable by parameter‡
Frequency Response		
	24 Kb/s	300 Hz to 2600 Hz ±3 dB
	32 Kb/s	300 Hz to 3400 Hz ±3 dB
	64 Kb/s	300 Hz to 3400 Hz ±3 dB
Audio Digitizing		
	24 Kb/s	OKI ADPCM @ 6 kHz sampling
	32 Kb/s	OKI ADPCM @ 8 kHz sampling
	64 Kb/s	G.711 PCM (µ-law for T-1 and A-law for E-1)
	48 Kb/s	G.711 PCM (µ-law for T-1 and A-law for E-1)
		MS WAV 11 kHz linear, 8- and 16-bit wave G.726 (32Kb/s-bit exact, and 16 Kb/s, 24 Kb/s, and 40 Kb/s bit rates)
		GSM (TIPHON, MSGSM)
	Digitization selection	Selectable by application on function call-by-call basis
Call Progress Analysis		
	Busy tone detection	Default setting designed to detect 74 out of 76 unique busy/congestion tones used in 97 countries as specified by CCITT Rec. E., Suppl. #2. Default uses both frequency and cadence detection. Application can select frequency only for faster detection in specific environments.
	Ring back detection	Default setting designed to detect 83 out of 87 unique ring back tones used in 96 countries as specified by CCITT Rec. E., Suppl. #2. Uses both frequency and cadence detection.
	Positive voice detection accuracy	>98% based on tests on a database of real world calls in North America
	Positive voice detection speed	Detects voice in as little as 1/10th of a second
	Positive answering machine detection	Standard
	Fax/modem detection	Preprogrammed
	Intercept detection	Detects entire sequence of the North American tri-tone. Other intercept tone sequences can be programmed
	Dial tone detection before dialing	Application enable/disable
		Supports up to three different user-definable dial tones
		Programmable dial tone drop out debouncing

Positive Answering Machine Detection / Positive Voice Detection: These performance results were measured using specific computer systems and/or components within specific lab environments and under specific system configurations. Any difference in system hardware, software design or configuration may affect actual performance. The results are furnished for informational use only and should not be construed as a commitment by Intel. Intel assumes no responsibility or liability for any errors or inaccuracies.

Outbound Dialing / Telemarketing: Outbound dialing systems may be subject to certain laws or regulations. Intel makes no representation that Intel products will satisfy the requirements of any such laws or regulations (including, without limitation, any regulations dealing with telemarketing).

Intel Model Name

DMV4802T1PCIHIZ for T-1 circuit line tap (two HiZ cable assemblies are supplied with each board)

DMV6002E1PCIHIZ for E-1 circuit line tap (two HiZ cable assemblies are supplied with each board)

Hardware System Requirements

Intel® Pentium® III processor or higher class IBM AT PC bus or compatible computer recommended

Operating system and memory requirements vary according to the number of channels being used per system. (Only Windows NT 4.0, Windows 2000, or Windows XP operating systems are currently supported with this product.)

Check the documentation for the System Release you are using for further information:
http://resource.intel.com/telecom/support/documentation/releases/index.htm

Additional Components (with Item Market Name)

- Multi-drop CT Bus cables (CBLCTB68C3DROP, CBLCTB68C4DROP, CBLCTB68C8DROP, CBLCTB68C12DROP, CBLCTB68C16DROP)
- CT Bus/SCbus adapter (CTBUSTOSCBUSADP)

To learn more, visit our site on the World Wide Web at **http://www.intel.com**.

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† Configurable to meet country-specific PTT requirements. Actual specification may vary from country to country for approved products.

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