DataKinetics

System7

PCCS6
User Manual

DataKinetics Ltd Fordingbridge Hants England Tel: +44 (0)1425 655050 Fax: +44 (0)1425 655075

Revision History

Issue	Date	Changes
1	07-Jan-97	

IMPORTANT INFORMATION

The information in this manual is supplied without warranty as to its accuracy. DataKinetics is not responsible or liable for any loss or damage of whatever kind arising from the use of the PCCS6 and it supporting software and documentation.

Sections of this manual describing the MVIP Bus and functions to control this bus are extracted from the Multi-Vendor Integration Protocol Reference Manual Release 1.0, which is copyright Natural MicroSystems Corporation.

MVIP, MVIP Bus and Multi-Vendor Integration Protocol are trademarks of Natural MicroSystems Corporation.

ST-BUS is a trademark of Mitel Corporation.

SCSA and **SCbus** are trademarks of Dialogic Corporation

CONTENTS

1. OVERVIEW

1.1 INTRODUCTION

The PCCS6 is a Signalling System No. 7 interface card for PC bus computers. It provides the Message Transfer Part for up to three signalling links.

The board physically occupies a single slot in the host PC and communicates with the host using a dual port memory interface which appears in the PC's memory address space.

The base I/O address of the card may be changed to avoid clashes with other cards installed in the PC and to allow multiple PCCS6s to be installed. The board does not require any DMA channels.

Two PCM expansion connectors are provided for the connection of third party cards such as voice processing and fax cards. The MVIP connector is compatible with the MVIP digital telephony bus. The SCbus connector is compatible with Dialogic SCSA.

This manual describes the physical properties of the board including the boards specification, the installation procedure and all option link settings. The user should refer to the Programmer's Maunal for the appropriate operating system for details of the software that runs on the board.

1.2 SPECIFICATIONS

1.2.1 Trunk interface

CEPT (E1) version (unbalanced) ..... 2048 kbit/s 75 Ohm
CEPT (E1) version (balanced) ..... 2048 kbit/s 120 Ohm
T1 version ..... 1544 kbit/s 100 Ohm

The board is available with one or two trunk interfaces.

1.2.2 Serial Ports

Electrical ..... V11/RS422 (V35 compatible)
Synchronous speeds ..... 4.8 kbit/s to 64 kbit/s

1.2.3 Signalling Interface

Trunk interface and MVIP bus

Signalling bit rate ..... 64 kbit/s or 56 kbit/s
Timeslot ..... Up to 3, programmable
Clock source ..... on-board oscillator, trunk interface, MVIP bus or SCbus

Serial ports

Signalling bit rate ..... 4.8 kbit/s to 64 kbit/s

1.2.4 PC Bus Interface

4kbyte dual-port memory, mappable on any 4k boundary from 80000h to FF000h.

4 consecutive I/O locations, mappable on any 4byte boundary from 000h to 3FCh.

Interrupt selectable from IRQ3-7, 9-15, multiple boards share the same interrupt. (The DOS driver will also work in polled mode, using no interrupts)

1.2.5 Physical

Full-length ISA card, 16-bit connector

1.2.6 Power requirements

+5v 1.5A

1.3 SYSTEM REQUIREMENTS

To use the PCCS6, your computer must meet the following minimum specification:

1.3.1 Hardware

- IBM PC, PC/XT, PC/AT or compatible
- One free 16 bit expansion slot

1.4 RELATED DOCUMENTATION

For further information on the SCbus, refer to the Dialogic SCSA Hardware Model Specification. This document is available from Dialogic Corporation, 300 Littleton Road, Parsippany, NJ 07054, USA.

For further information on the ST-Bus, refer to the MITEL Corporation Application Note MSAN-126.

For further information on the MVIP bus, refer to the Multi-Vendor Integration Protocol Reference Manual. This document is available from Natural MicroSystems Corporation, 8 Erie Drive, Natick, MA 01760-1339, USA..

2. HARDWARE INSTALLATION

2.1 UNPACKING THE PCCS6

The PCCS6 is supplied in an anti-static bag and should always be stored in its anti-static bag when not installed in a computer. The PCCS6 is susceptible to damage from static electricity and should always be handled accordingly.

Before installing the PCCS6, you will need to check the switch and jumper settings for your required configuration.

2.2 PCCS6 JUMPER SETTINGS

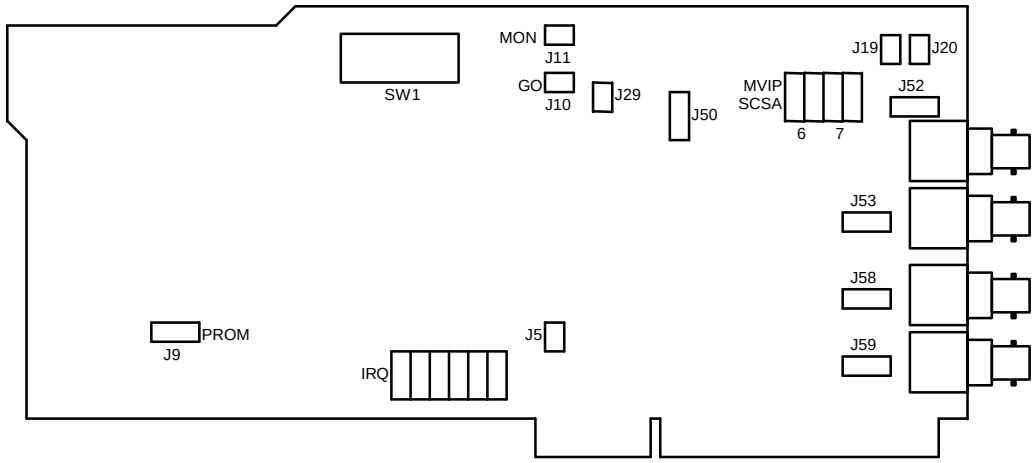

Fig. 2.1 Jumper positions

There are a number of jumpers which allow the board to be configured. The jumper positions are shown in figure 2.1.

2.2.1 Board I/O Address (SW1)

Used to select one of 256 possible I/O base addresses for the PCCS6. The board occupies 4bytes of I/O space mappable on 4 byte boundaries from 000h to 3FCh. The I/O address corresponding to each switch setting is shown in Fig. 2.2.

SW1 87654321	Address (hex)	SW1 87654321	Address (hex)	SW1 87654321	Address (hex)	SW1 87654321	Address (hex)
□□□□□□□□	000	□□■□□□□□	080	□■□□□□□□	100	□■■□□□□□	180
□□□□□□□■	004	□□■□□□□■	084	□■□□□□□■	104	□■■□□□□■	184
□□□□□□■□	008	□□■□□□■□	088	□■□□□□■□	108	□■■□□□■□	188
□□□□□□■■	00C	□□■□□□■■	08C	□■□□□□■■	10C	□■■□□□■■	18C
□□□□□■□□	010	□□■□□■□□	090	□■□□□■□□	110	□■■□□■□□	190
□□□□□■□■	014	□□■□□■□■	094	□■□□□■□■	114	□■■□□■□■	194
□□□□□■■□	018	□□■□□■■□	098	□■□□□■■□	118	□■■□□■■□	198
□□□□□■■■	01C	□□■□□■■■	09C	□■□□□■■■	11C	□■■□□■■■	19C
□□□□■□□□	020	□□■□■□□□	0A0	□■□□■□□□	120	□■■□■□□□	1A0
□□□□■□□■	024	□□■□■□□■	0A4	□■□□■□□■	124	□■■□■□□■	1A4
□□□□■□■□	028	□□■□■□■□	0A8	□■□□■□■□	128	□■■□■□■□	1A8
□□□□■□■■	02C	□□■□■□■■	0AC	□■□□■□■■	12C	□■■□■□■■	1AC
□□□□■■□□	030	□□■□■■□□	0B0	□■□□■■□□	130	□■■□■■□□	1B0
□□□□■■□■	034	□□■□■■□■	0B4	□■□□■■□■	134	□■■□■■□■	1B4
□□□□■■■□	038	□□■□■■■□	0B8	□■□□■■■□	138	□■■□■■■□	1B8
□□□□■■■■	03C	□□■□■■■■	0BC	□■□□■■■■	13C	□■■□■■■■	1BC
□□□■□□□□	040	□□■■□□□□	0C0	□■□■□□□□	140	□■■■□□□□	1C0
□□□■□□□■	044	□□■■□□□■	0C4	□■□■□□□■	144	□■■■□□□■	1C4
□□□■□□■□	048	□□■■□□■□	0C8	□■□■□□■□	148	□■■■□□■□	1C8
□□□■□□■■	04C	□□■■□□■■	0CC	□■□■□□■■	14C	□■■■□□■■	1CC
□□□■□■□□	050	□□■■□■□□	0D0	□■□■□■□□	150	□■■■□■□□	1D0
□□□■□■□■	054	□□■■□■□■	0D4	□■□■□■□■	154	□■■■□■□■	1D4
□□□■□■■□	058	□□■■□■■□	0D8	□■□■□■■□	158	□■■■□■■□	1D8
□□□■□■■■	05C	□□■■□■■■	0DC	□■□■□■■■	15C	□■■■□■■■	1DC
□□□■■□□□	060	□□■■■□□□	0E0	□■□■■□□□	160	□■■■■□□□	1E0
□□□■■□□■	064	□□■■■□□■	0E4	□■□■■□□■	164	□■■■■□□■	1E4
□□□■■□■□	068	□□■■■□■□	0E8	□■□■■□■□	168	□■■■■□■□	1E8
□□□■■□■■	06C	□□■■■□■■	0EC	□■□■■□■■	16C	□■■■■□■■	1EC
□□□■■■□□	070	□□■■■■□□	0F0	□■□■■■□□	170	□■■■■■□□	1F0
□□□■■■□■	074	□□■■■■□■	0F4	□■□■■■□■	174	□■■■■■□■	1F4
□□□■■■■□	078	□□■■■■■□	0F8	□■□■■■■□	178	□■■■■■■□	1F8
□□□■■■■■	07C	□□■■■■■■	0FC	□■□■■■■■	17C	□■■■■■■■	1FC

□ = switch on ■ = switch off

Fig. 2.2a Board base address

SW1 87654321	Address (hex)	SW1 87654321	Address (hex)	SW1 87654321	Address (hex)	SW1 87654321	Address (hex)
■□□□□□□□	200	■□■□□□□□	280	■■□□□□□□	300	■■■□□□□□	380
■□□□□□□■	204	■□■□□□□■	284	■■□□□□□■	304	■■■□□□□■	384
■□□□□□■□	208	■□■□□□■□	288	■■□□□□■□	308	■■■□□□■□	388
■□□□□□■■	20C	■□■□□□■■	28C	■■□□□□■■	30C	■■■□□□■■	38C
■□□□□■□□	210	■□■□□■□□	290	■■□□□■□□	310	■■■□□■□□	390
■□□□□■□■	214	■□■□□■□■	294	■■□□□■□■	314	■■■□□■□■	394
■□□□□■■□	218	■□■□□■■□	298	■■□□□■■□	318	■■■□□■■□	398
■□□□□■■■	21C	■□■□□■■■	29C	■■□□□■■■	31C	■■■□□■■■	39C
■□□□■□□□	220	■□■□■□□□	2A0	■■□□■□□□	320	■■■□■□□□	3A0
■□□□■□□■	224	■□■□■□□■	2A4	■■□□■□□■	324	■■■□■□□■	3A4
■□□□■□■□	228	■□■□■□■□	2A8	■■□□■□■□	328	■■■□■□■□	3A8
■□□□■□■■	22C	■□■□■□■■	2AC	■■□□■□■■	32C	■■■□■□■■	3AC
■□□□■■□□	230	■□■□■■□□	2B0	■■□□■■□□	330	■■■□■■□□	3B0
■□□□■■□■	234	■□■□■■□■	2B4	■■□□■■□■	334	■■■□■■□■	3B4
■□□□■■■□	238	■□■□■■■□	2B8	■■□□■■■□	338	■■■□■■■□	3B8
■□□□■■■■	23C	■□■□■■■■	2BC	■■□□■■■■	33C	■■■□■■■■	3BC
■□□■□□□□	240	■□■■□□□□	2C0	■■□■□□□□	340	■■■■□□□□	3C0
■□□■□□□■	244	■□■■□□□■	2C4	■■□■□□□■	344	■■■■□□□■	3C4
■□□■□□■□	248	■□■■□□■□	2C8	■■□■□□■□	348	■■■■□□■□	3C8
■□□■□□■■	24C	■□■■□□■■	2CC	■■□■□□■■	34C	■■■■□□■■	3CC
■□□■□■□□	250	■□■■□■□□	2D0	■■□■□■□□	350	■■■■□■□□	3D0
■□□■□■□■	254	■□■■□■□■	2D4	■■□■□■□■	354	■■■■□■□■	3D4
■□□■□■■□	258	■□■■□■■□	2D8	■■□■□■■□	358	■■■■□■■□	3D8
■□□■□■■■	25C	■□■■□■■■	2DC	■■□■□■■■	35C	■■■■□■■■	3DC
■□□■■□□□	260	■□■■■□□□	2E0	■■□■■□□□	360	■■■■■□□□	3E0
■□□■■□□■	264	■□■■■□□■	2E4	■■□■■□□■	364	■■■■■□□■	3E4
■□□■■□■□	268	■□■■■□■□	2E8	■■□■■□■□	368	■■■■■□■□	3E8
■□□■■□■■	26C	■□■■■□■■	2EC	■■□■■□■■	36C	■■■■■□■■	3EC
■□□■■■□□	270	■□■■■■□□	2F0	■■□■■■□□	370	■■■■■■□□	3F0
■□□■■■□■	274	■□■■■■□■	2F4	■■□■■■□■	374	■■■■■■□■	3F4
■□□■■■■□	278	■□■■■■■□	2F8	■■□■■■■□	378	■■■■■■■□	3F8
■□□■■■■■	27C	■□■■■■■■	2FC	■■□■■■■■	37C	■■■■■■■■	3FC

□ = switch on ■ = switch off

Fig. 2.2b Board base address

If in doubt, refer to your PC manual and the manuals for any other expansion cards to check which I/O address range will avoid clashes with existing cards.

2.2.2 IRQ

Used to select which interrupt line the PCCS6 will use. The IRQ numbers are marked on the appropriate links. Only one of these links should be fitted. Note that there is a spare link position for jumper storage if interrupts are not used.

2.2.3 MVIP/SCSA selection (J43, J44, J45 & J46)

Used to select the source of data for streams 6 and 7 of the cross connect switch, the data can come from either the MVIP bus or the SCbus daughtercard. Normally fitted in the SCSA position for use with the SCbus daughtercard and MVIP position for use with MVIP.

2.2.4 TX Screen Trunk Interface 1 (J52)

This link is only presend on versions of the board which use BNC connectors.

When fitted, connects the shell of the BNC output connector to the on-board 0V rail. This link is usually fitted.

2.2.5 RX Screen Trunk Interface 1(J53)

This link is only presend on versions of the board which use BNC connectors.

When fitted, connects the shell of the BNC input connector to the on-board 0V rail. This link is **not** usually fitted.

2.2.6 TX Screen Trunk Interface 2 (J58)

This link is only presend on versions of the board which use BNC connectors.

When fitted, connects the shell of the BNC output connector to the on-board 0V rail. This link is usually fitted.

2.2.7 RX Screen Trunk Interface 2(J59)

This link is only presend on versions of the board which use BNC connectors.

When fitted, connects the shell of the BNC input connector to the on-board 0V rail. This link is **not** usually fitted.

2.2.8 MVIP C2 Termination (J19)

When fitted, provides the optional termination of the C2 clock line in accordance with the MVIP specification. **If no other boards are connected to the PCM highway, the state of this link is not significant.** Refer to section 2.5 for further information

2.2.9 MVIP /C4 Termination (J20)

When fitted, provides the optional termination of the /C4 clock line in accordance with the MVIP specification. **If no other boards are connected to the PCM highway, the state of this link is not significant.** Refer to section 2.5 for further information.

2.2.10 Factory fitted links

The following links are factory fitted and would not normally need to be changed.

J5	Not fitted
J9 (PROM)	Fitted in 128 position
J10 (GO)	Fitted
J11 (MON)	Not fitted
J50	Position A

2.3 INSTALLATION

Before installing the card, refer to the appropriate Appendix for safety instructions.

Any jumper positions not listed above are for test purposes only and no jumpers should be fitted to these positions.

After setting the jumpers and the address switch, the card can be inserted into the PC expansion slot.

CAUTION

To avoid electrical shock, make sure that the computer is switched off and **disconnected from the mains supply** before removing the cover from the computer. Cards should never be fitted to or removed from the computer while the power is on.

Having ensured that all power is off and the power lead disconnected, remove the cover from the PC. Consult your computer manual for the appropriate instructions.

Select a vacant expansion slot. (If in doubt, refer your computer manual for advice).

If a blanking plate is fitted, remove it by undoing the retaining screw at the top of the blanking plate and then removing the plate. Save the screw for holding the PCCS6 in place. You may wish to retain the blanking plate for possible future use.

Ensure that the edge connector on the PCCS6 is aligned with the expansion slot connector in the PC and press the PCCS6 into place. Secure the PCCS6 using the screw that was removed from the expansion slot cover.

If you are connecting other cards to the MVIP Bus connector, refer to section 2.5 for further information on the MVIP Bus.

Now replace the cover of the PC. Reconnect the mains supply and switch on the PC.

Once the PCCS6 is installed, move on to the section on software installation in the DataKinetics Programmer's Manual for the operating system you are using.

2.4 SERIAL PORTS

The PCCS6 has an optional serial daughtercard to provide two serial ports, Port A and Port B, which may be used for up to two of the three signalling links instead of timeslots on the trunk interface, MVIP bus or SCbus.

When used for signalling, the serial ports are used in synchronous mode. The serial clock may be sourced from the on-board clock generator or an external clock. Note that in both cases the same clock is used for transmit and receive data, i.e. separate transmit and receive clocks are not used.

For internal clock operation use the transmit clock pins and make no connection to the receive clock pins on the 26-way D-type connector.

For external clock operation connect the clock source to the receive clock pins on the 26-way D-type connector and make no connection to the transmit clock pins.

2.5 MVIP BUS

2.5.1 Overview

The PCCS6 is fitted with a 40 way header on the top edge of the card which conforms to the MVIP Bus standard. This bus may be used to connect other MVIP compatible cards to the PCCS6, such as voice processing and fax cards or further PCCS6 cards.

The MVIP Bus consists of 16 2.048Mbit/s data streams with associated clock and framing signals. These signals adhere to the Mitel ST-Bus Generic Device Specification (Rev. A), as specified in the Mitel Application Note MSAN-126. The signals are carried between cards in a PC chassis using a 40 way ribbon cable. The maximum ribbon cable length is 22 inches.

2.5.2 Signal Definitions

For the pin-out of the MVIP connector, refer to section 2.7. The following signal description is an extract from the MVIP Reference Manual.

/C4 and C2 are the Mitel ST-Bus 4.096 MHz and 2.048 MHz clocks. /F0 is the Mitel ST-Bus 8 kHz framing signal. DSi0 thru DSi7 and DSo0 thru DSo7 are 2.048 Mbit/s serial data streams conforming to the Mitel ST-Bus serial data stream specifications. SEC8K is a secondary 8 kHz signal line used to carry 8 kHz timing information derived from trunks on a secondary or subsequent digital trunk interface to a digital trunk interface board that is providing clocks to the MVIP Bus.

2.5.3 Signal Conventions

The following is an extract from the MVIP Reference Manual.

In principal the sixteen serial data streams can be used independently. However, in MVIP systems the data streams are normally paired to provide full-duplex 64 kbit/s voice or data paths. By convention, DSi0 thru DSi7 carry data coming in from the telephone network and DSo0 thru DSo7 carry data going out to the telephone network.

2.5.4 MVIP Clock Signals

The clock lines C2 and /C4 must be electrically terminated. All MVIP cards should provide this termination on a jumper-selectable basis. (Refer to section 2.2 for jumper settings).

For systems with five or fewer MVIP Bus connections and less than 90 pF load on the clock lines, it is adequate to place the circuit board that is the master clock source at one end of the MVIP cable and provide the termination on the board which is physically at the other end of the cable.

On systems with more than five MVIP connections or more than 90 pF of load on the clock lines, both ends of the cable should be terminated.

2.6 SCbus

2.6.1 Overview

The PCCS6 is fitted with an (optional) daughtercard containing the SCbus interface providing a 26 way header on the top edge of the card which conforms to the Dialogic SCbus specification. This bus may be used to connect other SCbus compatible cards to the PCCS6, such as voice processing and fax cards or further PCCS6 cards.

The SCbus consists of 16 4096Kbit/s data streams with associated clock and framing signals. The sixteen serial data streams can be used independently and timeslots on individual streams may be grouped to provide a higher bandwidth data path. The signals are carried between cards in a PC chassis using a 26 way ribbon cable. The maximum ribbon cable length is 21 inches.

2.7 CONNECTORS

2.7.1 Trunk interface ports

2.7.1.1 Unbalanced version

The CEPT unbalanced trunk interface version is fitted with 75Ω BNC connectors, the two connectors nearest the top of the card are the first port and the two connectors nearest the bottom of the card are the second port. The top connector of each pair is the output.

2.7.1.2 Balanced version

The CEPT balanced trunk interface and T1 versions are fitted with a female RJ45 connector. The connector pin-out and signal descriptions are shown in Fig. 2.4.

Pin No	Direction	Function
1	Input	Receive tip
2	Input	Receive ring
3		GND
4	Output	Transmit tip
5	Output	Transmit ring
6		GND
7		No connection
8		No connection

Fig. 2.4 Balanced trunk interface connector pin-out

2.7.2 Serial ports (Port 12)

Connection to the V11 or V28 signalling links is made via the female 26 way 'D' connector fitted to the PCCS6 serial port daughtercard. The connector pin-out and signal descriptions are shown in Fig. 2.5.

Pin No	Direction	Function
1		Chassis
2	Output	V11 Transmit inverted clock Port B
3	Output	V11 Transmit clock Port B
4	Output	V11 Transmit inverted data Port B
5	Output	V11 Transmit true data Port B
6	Input	V11 Receive inverted clock Port B
7	Input	V11 Receive clock Port B
8	Input	V11 Receive inverted data Port B
9	Input	V11 Receive true data Port B
10		Signal Ground
11	Input	V28 Receive data Port B
12	Output	V28 Transmit data Port B
13		Do not connect
14		Do not connect
15		Do not connect
16		Do not connect
17		Do not connect
18		Do not connect
19	Output	V11 Transmit inverted clock Port A
20	Output	V11 Transmit clock Port A
21	Output	V11 Transmit inverted data Port A
22	Output	V11 Transmit true data Port A
23	Input	V11 Receive inverted clock Port A
24	Input	V11 Receive clock Port A
25	Input	V11 Receive inverted data Port A
26	Input	V11 Receive true data Port A

Fig. 2.5 Serial port connector pin-out

2.7.3 MVIP Bus connector (Port 6)

Pin No	Signal	Pin No	Signal
1	RESERVED	2	RESERVED
3	RESERVED	4	RESERVED
5	RESERVED	6	RESERVED
7	DSo0	8	DSi0
9	DSo1	10	DSi1
11	DSo2	12	DSi2
13	DSo3	14	DSi3
15	DSo4	16	DSi4
17	DSo5	18	DSi5
19	DSo6	20	DSi6
21	DSo7	22	DSi7
23	RESERVED	24	RESERVED
25	RESERVED	26	RESERVED
27	RESERVED	28	RESERVED
29	RESERVED	30	GROUND
31	/C4	32	GROUND
33	/F0	34	GROUND
35	C2	36	GROUND
37	SEC8K	38	GROUND
39	RESERVED	40	RESERVED

Fig. 2.6 MVIP connector pin-out

2.7.4 SCbus connector (Port 10)

Pin No	Signal	Description
1	SCLKx2*	Twice the frequency of SCLK.
2	GND	
3	SCLK	System clock.
4	Reserved	
5	FSYNC*	Frame sync pulse.
6	CLKFAIL	Clock fail, active high.
7	SD0	Bidirectional data stream.
8	GND	
9	SD1	Bidirectional data stream.
10	SD2	Bidirectional data stream.
11	SD3	Bidirectional data stream.
12	SD4	Bidirectional data stream.
13	SD5	Bidirectional data stream.
14	SD6	Bidirectional data stream.
15	GND	
16	SD7	Bidirectional data stream.
17	SD8	Bidirectional data stream.
18	SD9	Bidirectional data stream.
19	SD10	Bidirectional data stream.
20	SD11	Bidirectional data stream.
21	GND	
22	SD12	Bidirectional data stream.
23	SD13	Bidirectional data stream.
24	SD14	Bidirectional data stream.
25	SD15	Bidirectional data stream.
26	MC	Message channel.

Fig. 2.7 SCbus connector pin-out

APPENDIX A

COUNTRY-SPECIFIC INFORMATION (UK)

A.1 INTRODUCTION

This appendix contains information on the use of the PCCS6 which is specific to the UK.

A.2 SAFETY

A.2.1 Overview

The PCCS6 complies with CENELEC specifications EN41003 and EN60950. To maintain compliance with these specification, it is essential that the instructions in this appendix are complied with.

A.2.2 Host PC

The PCCS6 must only be installed in a PC which provides an SELV host environment as defined in EN60950 (“the Host”.)

A.2.3 Power supply

It is a requirement that the total power required by the Host, all installed adapter cards including PCCS6s and any other equipment drawing power from the Host must be within the power supply specification of the Host. The power requirements for the PCCS6 are specified in the User Manual of which this appendix forms part.

A.2.4 Other expansion cards

It is a requirement that if other installed adapter cards use or generate a hazardous voltage, minimum creepage and clearance distances are maintained as specified in the table below. A hazardous voltage for the purposes of this document is one which exceeds 42.4V peak ac or 60V dc. If you have any doubt, seek advice from a competent engineer before installing other adapters in the Host.

A.2.5 Clearance and creepage distances

The PCCS6 must be installed such that, with the exception of connections to the Host, clearance and creepage distances shown in the table below are maintained between the PCCS6 and any other assemblies which use or generate a voltage as shown in the table. The larger distances shown in brackets apply where the local environment within the Host is subject to conductive pollution or dry non-conductive pollution which could become conductive due to condensation.

Voltage used or generated by the Host or other adapter cards	**Clearance (mm)**	**Creepage (mm)**
Up to 50 v_{rms} or v_{dc}	2.0	2.4 (3.8)
Up to 125 v_{rms} or v_{dc}	2.6	3.0 (4.8)
Up to 250 v_{rms} or v_{dc}	4.0	5.0 (8.0)
Up to 300 v_{rms} or v_{dc}	4.0	6.4 (10.0)
Over 300 v_{rms} or v_{dc}	For a Host or other adapter card fitted in the Host using or generating voltages greater than 300 v_{rms} or v_{dc}, advice from a competent telecommunications safety engineer must be obtained before installation of the relevant equipment.	

Table A.1 Clearance and creepage distance values

Clearance and creepage distances are measured as shown in Figure 1 between the PCCS6 and any other assemblies which use or generate a hazardous voltage as shown in Table A.1.

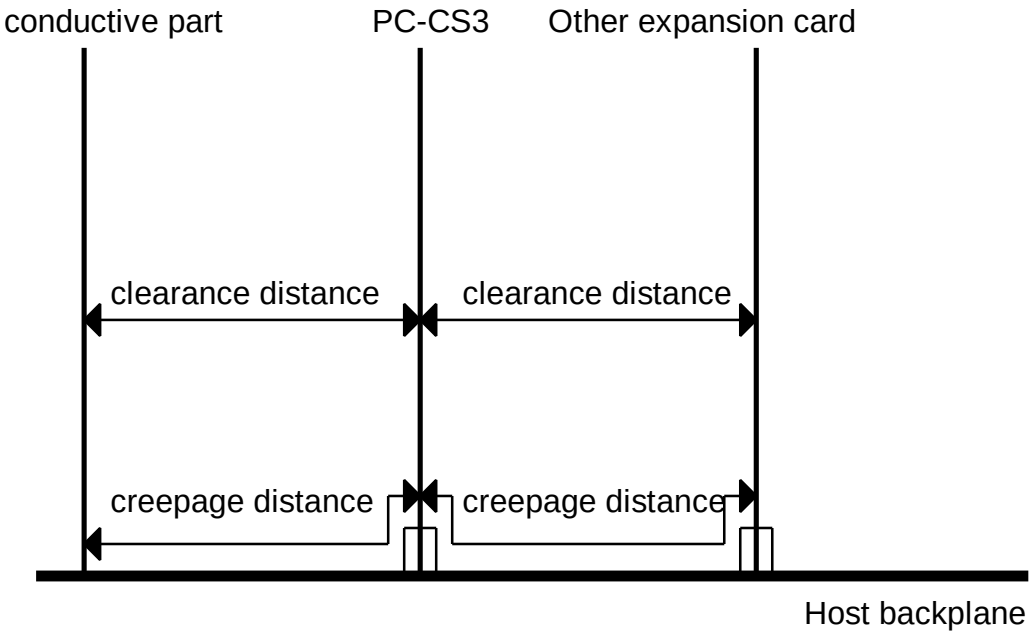

Figure A.1 Clearance and creepage distance measurement

A.2.6 Connectors

The safety status of the connectors on the PCCS6 used to interface to other equipment is shown in Table A.2.

Port	Type	Description	Status
1, 2, 3 & 4	BNC or RJ45	Trunk Interface	TNV normally operating within SELV limits
6	40 way IDC box header	MVIP Bus	SELV
7	Gold plated PCB finger connector	ISA Bus	SELV
10	26 way IDC box header on daughter board	SC Bus	SELV
12	26 way D-type on daughter board	Serial Port	SELV

Table A.2 Safety status of ports